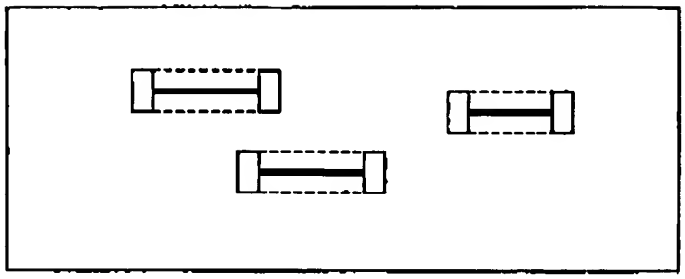
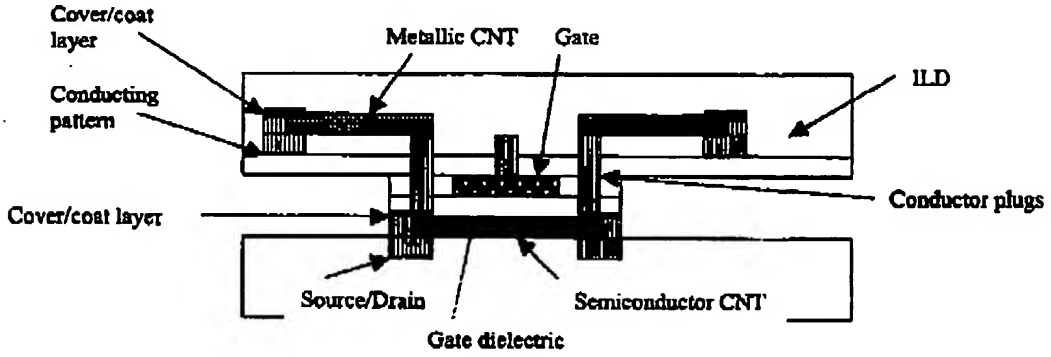


d) deposition of gate dielectric and gate followed by litho etch to form transistors and remove unwanted conductive pattern with SW CNT's



e) similar operations to described above are done with metallic SW CNT's to form conductors and interconnect SW CNT's devices. Vias/Contacts are filled with metals. Vertical integration of layer containing SW CNT's devices is possible (as thin film stack)

Figure 2. Vertical cross-section of SW CNT's transistor (single channel and multichannel devices)

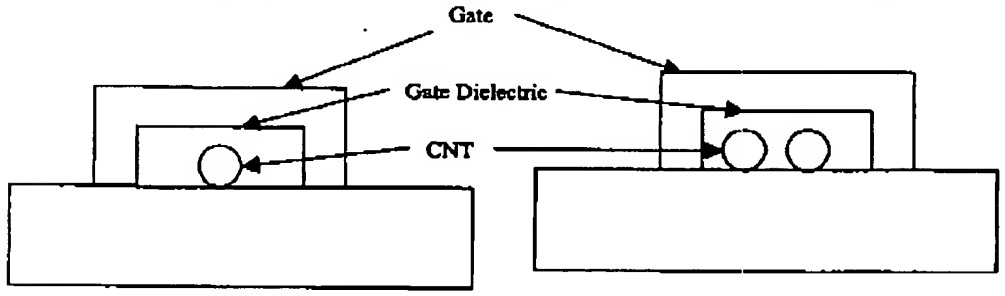


EXHIBIT 1